Industry Day Theme #1 {Clean Energy for Sustainable Economy and Environment}

Design Consideration in SiC Based High Frequency Converters

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Abstract

- SiC power devices have the advantage of faster switching capability, resulting in low switching losses compared to its Si counterpart. However parasitic inductance due to converter layout and load parasitic capacitance, affects the switching performance of the device.
- In presence of such parasitics and high di/dt and dv/dt due to faster switching, the device experiences huge voltage and current overshoot during switching transient which leads to failure of the device.
- This work presents an improved interconnect layout of the DC link capacitor to minimize parasitic inductance. Further, the effect of SiC Schottky barrier diode (SBD) on switching loss in different phase leg configuration was investigated.

Introduction

- Wide-band gap devices like Silicon Carbide (SiC) or Gallium Nitride (GaN) MOSFET can be switched five to ten times faster than widely used Silicon (Si) IGBT.
- SiC converters operate at high switching frequency which enables the use of smaller filter inductor and capacitor. This drastically reduces the converter form factor thereby increasing volumetric efficiency.
- The switching and conduction losses associated with SiC devices are very low, leading to high electrical efficiency.
- SiC MOSFET has better thermal stability, higher breakdown field strength and low on-state resistance than its Si counterpart.
- At fast switching transition i.e. at high di/dt and dv/dt, there are challenges that needs attention. Most prominent is the high voltage and current stress that the device experience during transient due to the presence of parasitic inductance of converter layout and load capacitance. This undesired voltage and current stress increases switching losses and eventually leads to failure of the device.
- This work is focused to minimize parasitic inductance by improving interconnect layout of DC link capacitor bank and reducing its effect on the switching performance of SiC MOSFET.
- Effect of SBD when used as an external freewheeling diode along with SiC MOSFET was also investigated. Different phase leg configuration has been made for comparing the switching losses.

Experimental Setup

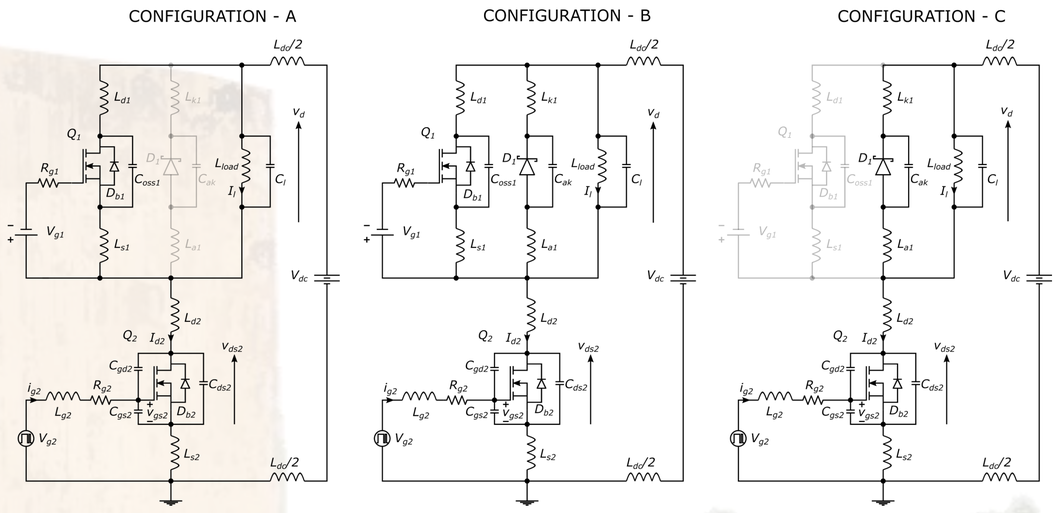

Fig. 1: Schematic of double pulse test in different phase leg configuration

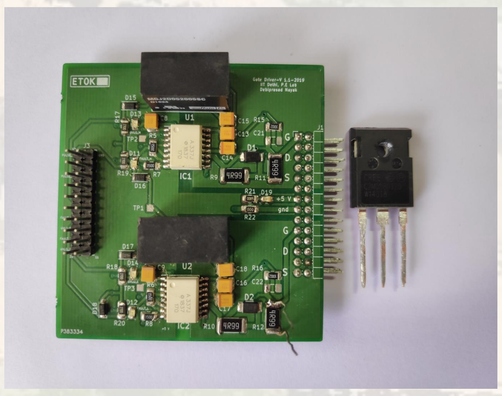

Fig. 2: Dual channel isolated SiC MOSFET gate driver

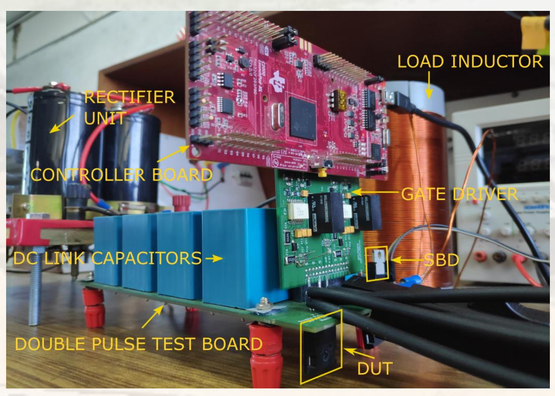

Fig. 3: Test setup

Industrial Significance

SiC based converters has high electrical and volumetric efficiency and such converters can be used in variety of applications. Electric vehicle drive, charging station, integration of renewable energy to existing grid are the few areas where high power density converters could play a major role in reducing the solution size and increasing the overall system efficiency.

Technology Readiness Level

Currently we are able to deliver power of 1.5 kW at 600 V DC bus and 100 kHz switching frequency. We have the capability of developing high power SiC based converter.

Result

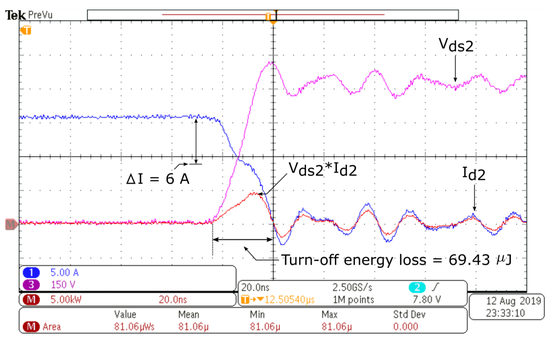

Fig. 4: Energy loss during turn-off

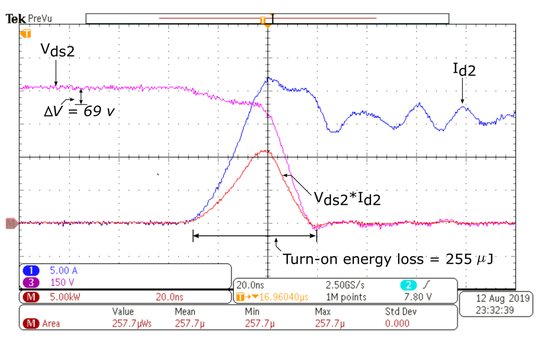

Fig. 5: Energy loss during turn-on

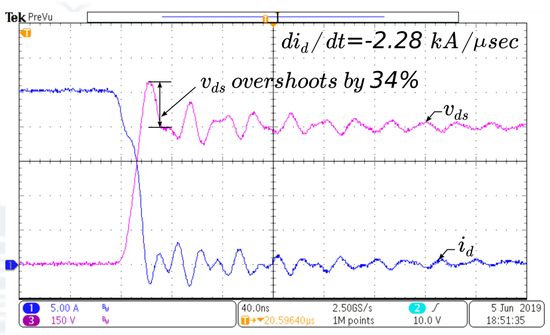

Fig. 6: Turn-off in conventional layout

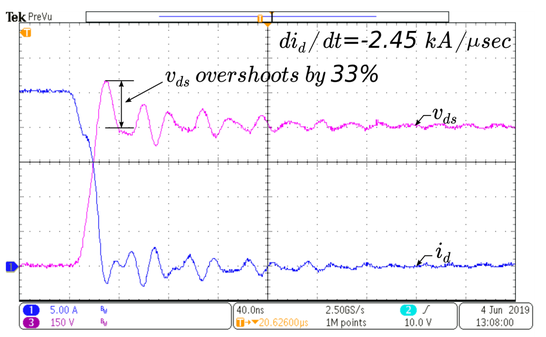

Fig. 7: Turn-off in improved layout

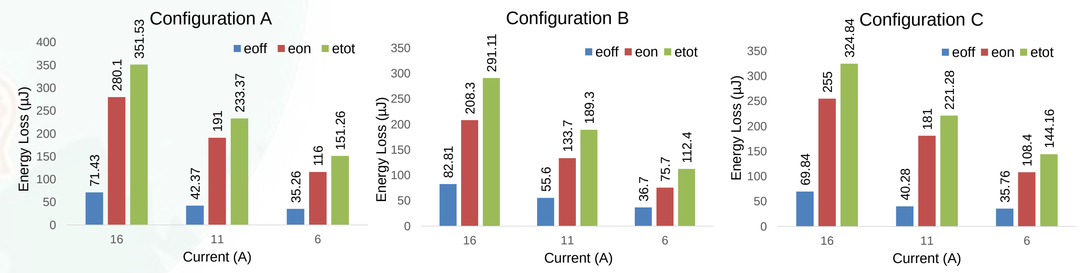

Fig. 8: Switching loss comparison for different phase leg configuration

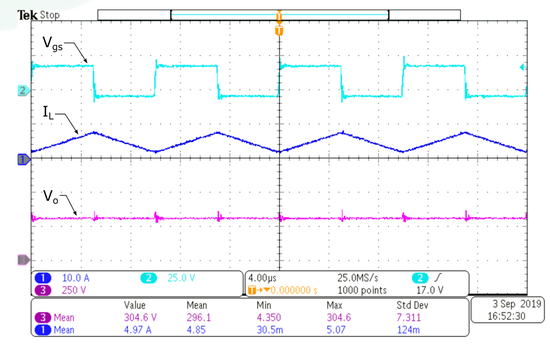

Fig. 9: Output waveforms for 1.5 kw buck converter

Fig. 10: Thermal image of SiC MOSFET running at 100 kHz

Conclusions

This work presents an improved interconnect layout of the DC link capacitor to minimize DC bus parasitic inductance. It was observed that if capacitor bank are connected, which provides reverse coupling between adjacent leg, the parasitic inductance can be reduced by 8.79%. The parasitic inductance of the power loop can be further reduced by increasing the number of leg in the DC link capacitor bank. Further the switching losses on this improved interconnect layout were investigated in different phase leg configuration by conducting the clamped inductive load test. It was observed that the inclusion of SiC SBD as a free-wheeling anti-parallel diode along with SiC MOSFET reduces the total switching energy loss by 7.6 %. Switching loss was further reduced to 17.2 % when only SiC SBD was used as a free-wheeling diode.

References

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Acknowledgement

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